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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/714,243	11/13/2003	Bomy Chen	2102397-992740	2456

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EXAMINER	
NGUYEN, DAO H	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 09/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/714,243	CHEN ET AL.	
	Examiner	Art Unit	
	Dao H. Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *20-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1103 & 0804*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the communications dated 11/13/2003 through 08/31/2005.

Claims 1-24 are active in this application.

Acknowledges

2. Receipt is acknowledged of the following items from the Applicant.

a. Information Disclosure Statement (IDS) filed on 11/13/2003 and 08/10/2004. The references cited on the PTOL 1449 form have been considered.

Applicant is requested to cite any relevant prior art if being aware on form PTO-1449 in accordance with the guidelines set for in M.P.E.P. 609.

b. Applicant made a provisional election without traverse to prosecute the invention of Group I, claims 1-19, drawn to semiconductor devices. Affirmation of this election was made in the Response to Restriction Requirement, filed 08/31/2005.

Claims 20-24 have been withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a non-elected group there being no allowable generic or linking claim.

Applicant has the right to file a divisional application covering the subject matter of the non-elected claims.

Specification

3. The specification has been checked to the extent necessary to determine the presence of possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claim(s) 1-15 are rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent No. 5,616,510 to Wong.

Regarding claim 1, Wong discloses a non-volatile memory cell, as shown in figs. 5, 6, 14, 16, 20, 21, 23, and 25, comprising:

a substantially single crystalline substrate 2301 (fig. 23A-C, for example) of a first conductivity type (p-type, col. 20, lines 23-61) having a planar surface;

a trench 2307 (fig. 23A) in said planar surface, said trench 2307 having a side wall and a bottom;

a floating gate 2305 in said trench spaced apart and insulated from said sidewall and from said bottom (by gate dielectric 2308); said floating gate 2305 having a tip away from said bottom;

a first region 2302 of a second conductivity type (n-type) in said bottom;

a second region 2304 of a second conductivity type (n-type) along said planar surface, spaced apart from said first region 2302;

a channel region between said first region and said second region, said channel region along said sidewall;

a control gate 2309/2318 capacitively coupled to said floating gate 2305 and capable of effecting erase (col. 20, lines 31-61); and

a tunnel material 2308/2310 (fig. 23C) between said tip and said control gate 2309/2318.

Regarding claim 2, Wong discloses the memory cell wherein said tunnel material 2308/2310 is a tunnel oxide. See figs. 23 and col. 20, lines 23-61.

Regarding claim 3, Wong discloses the memory cell wherein said tunnel oxide permits Fowler-Nordheim tunneling of charges from said floating gate to said control

gate. This is inherent properties of floating gate transistor.

Regarding claim 4, Wong discloses the memory cell further comprising an insulation material 2308 between said floating gate 2305 and said sidewall of said trench 2307, said insulation material 2308 permitting injection of hot channel electrons from said channel region to said floating gate 2308 (properties of floating gate transistor). See figs. 23.

Regarding claim 5, Wong discloses an array of non-volatile memory cells, as shown in figs. 5, 6, 14, 16, 20, 21, 23, and 25, in a substantially single crystalline substrate 2301 (figs. 23A-C, for example) of a first conductivity type (p-type) having a planar surface, said array comprising:

a plurality of discontinuous trenches 2307 (fig. 23A) in said planar surface, spaced apart and substantially parallel to one another extending in a first direction; each of said discontinuous trenches 2307 having two sidewalls and a bottom and being discontinuous in said first direction by a plurality of isolations;

a first floating gate 2305 (along the one side of the trench) in each trench 2307 spaced apart and insulated from a first sidewall and from said bottom (by gate dielectric 2308); said first floating gate 2305 having a tip away from said bottom;

a second floating gate 2308 (along the other side of the trench) in each trench 2307 spaced apart and insulated from a second sidewall and from said bottom; said second floating gate 2307 having a tip away from said bottom;

a first region 2302 of a second conductivity type (n-type) in said bottom of each trench 2307;

a second region 2304 of said second conductivity type along said planar surface;

a channel region between each of said first region 2302 and said second region 2304, said channel region along said first and second sidewall;

a plurality of control gates 2309/2318, each control gate extending in a second direction, substantially perpendicular to said first direction, extending over a plurality of tips of a plurality of floating gates and insulated therefrom; and

a tunnel material 2310 between said plurality of tips and said control gate.

Regarding claim 6, Wong discloses the array wherein said tunnel material 2310 is a tunnel oxide. See figs. 23 and col. 20, lines 23-61.

Regarding claim 7, Wong discloses the array wherein said tunnel oxide permits Fowler-Nordheim tunneling of charges from said floating gates to said control gate. This is inherent properties of floating gate transistor.

Regarding claim 8, Wong discloses the array further comprising an insulation material 2308 between said first floating gate 2305 and said first sidewall of said trench,

said insulation material permitting injection of hot channel electrons from said channel region to said first floating gate (properties of floating gate transistor). See figs. 23.

Regarding claim 9, Wong discloses the array further comprising said insulation material 2308 between said second floating gate 2305 and said first sidewall of said trench, said insulation material permitting injection of hot channel electrons from said channel region to said second floating gate (properties of floating gate transistor). See figs. 23.

Regarding claim 10, Wong discloses a non-volatile memory device, as shown in figs. 5, 6, 14, 16, 20, 21, 23, and 25, in a substantially single crystalline substrate 2301 of a first conductivity type (p-type) having a planar surface, said device comprising:

an array of non-volatile memory cells arranged in a plurality of rows and columns (figs. 5-6, 14, 16, 20, 21, 25); wherein each cell comprising:

a trench 2307 (fig. 23A) in said planar surface, said trench 2307 having a side wall and a bottom;

a floating gate 2305 in said trench spaced apart and insulated from said sidewall and from said bottom (by gate dielectric 2308); said floating gate having a tip away from said bottom;

a first region 2302 of a second conductivity type (n-type) in said bottom;

a second region 2304 of a second conductivity type along said planar surface, spaced apart from said first region 2302;

a channel region between said first region 2302 and said second region 2304, said channel region along said sidewall;

a control gate 2309/2318 spaced apart from said tip and capacitively coupled to said tip; and

a tunnel material 2310 between said tip and said control gate; and

wherein cells in adjacent columns share a common trench to one side and a common second region to another side;

wherein cells in adjacent rows are separated by an isolation row (616 of fig. 6, or 1427 of fig. 14D, for example) and wherein said second region in one row is connected to said second region of another row (fig. 22); and;

wherein said control gate 2309/2318 of cells in the same row are connected together.

Regarding claim 11, Wong disclose the device wherein a control gate extends over a plurality of rows. See figs. 14, 22-233

Regarding claims 12-15, Wong discloses the array comprising all claimed limitations. See the rejections of claims 6-9.

Claim Rejections - 35 U.S.C. § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim(s) 16-19 is/are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 5,616,510 to Wong, in view of the following remarks.

Regarding claim 16, Wong discloses a circuit device, as shown in figs. 5, 6, 14, 16, 20, 21, 23, and 25, comprising:

a plurality of stacked gate non-volatile memory cells arranged in a plurality of rows and columns (figs. 16, 20, 22, 25); each cell having a first terminal 2302 and second terminal 2304 with a channel region therebetween, a floating gate 2305 spaced apart and insulated from said channel region, and a control gate 2309/2318 capacitively coupled with said floating gate 2305 to effect erasure;

wherein said cells in the same row are connected with each cell having a common second terminal 2304 with an adjacent cell to one side, and having a common first terminal 2302 with an adjacent cell to another side;

wherein cells in the same row have the control gate 2309 connected together; and

wherein cells in adjacent rows are separated by isolation (616 of fig. 6, or 1427 of fig. 14D, for example).

Wong is silent about a circuit device being a NAND circuit device.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made that the circuit device of Wong can be designed to be a NAND circuit device or any other desired circuit device, depending on the application of the device, since it would involve only routine skills in the art to form a NAND circuit device from disclosed transistors.

Regarding claim 17, Wong discloses the device wherein said first terminal 2302 is in a trench and said second terminal 2304 is not in a trench. See figs. 5-6, 14, 23.

Regarding claim 18, Wong discloses the device wherein said floating gate 2305 of cells in the same row are capacitively coupled to the same control gate. See figs. 14, 20-23.

Regarding claim 19, Wong discloses the device wherein cells in the same column have the same first terminal and the same second terminal. See figs. 14, 22-23.

Conclusion

8. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao H. Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday, 9:00 AM – 6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)272-1787. The fax numbers for all communication(s) is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.

David Nelms
Supervisory Patent Examiner
Technology Center 2800

Dao H. Nguyen
Art Unit 2818
September 4, 2005